DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Patrick L. Miller on 10/20/2009.

2. The application has been amended as follows:

- Claim 3 has been amended as following:

3. A method for adaptive clocking in a packet-based network between a first node and a second node, the method comprising:

receiving a first clock signal for transmission through the packet-based network at the first node;

repeatedly measuring, in a first phase, the first clock signal to obtain a plurality of frequency measurements of increasing accuracy at the first node;

determining a corresponding accuracy indicator for each frequency measurement at the first node, the accuracy indicator being a time duration of measurement;

individually transmitting each frequency measurement with its corresponding accuracy indicator through the packet-based network from the first node to the second node;

receiving each frequency measurement and corresponding accuracy indicator at the second node;

deriving, in the first phase, respective second clock signal signals from the frequency measurements and corresponding accuracy indicators at the second node,

~~substantially~~ to represent the first clock signal based on incremental converging of the second clock signals based on the received clock frequency measurements of increasing accuracy; and

transmitting the derived second clock signals signal from the second node to user equipment connected to the second node.

Allowable Subject Matter

3. Claims 1, 7, 8, 14,15; 2, 9, 10, 16, 17; 3, 11, 18; 4, 5, 6, 12, 13, 19, 20 renumbered 1 – 20 are allowed.

4. The following is an examiner's statement of reasons for allowance:

The prior art made of record, in single or in combination, fails to disclose explicitly the limitations of:

"a first node to take a plurality of clock frequency measurements of the first clock signal and to calculate corresponding accuracy indicators of the clock frequency measurements, each accuracy indicator being a time duration of measurement, and the clock frequency measurements being of increasing accuracy with respect to the first clock signal in a first phase of operation; a second node to receive the clock frequency measurements and corresponding accuracy indicators and to synthesize respective second clock signals based on the clock frequency measurements and corresponding accuracy indicator indicators; and a packet-based network to transmit the clock frequency measurements and corresponding accuracy indicators from the first node to the second node, wherein, in the first phase of operation, the synthesis of the second clock signals involves incremental convergence of the second clock signals toward the first clock signal based on the received clock frequency measurements of increasing accuracy" as disclosed in claim 1.

"a first node to receive the bit synchronous data for transmission through the packet-based network, the first node including measurement hardware to generate a plurality of clock frequency measurements based on a first clock signal received by the first node and a corresponding accuracy indicator for each of the clock frequency measurements, the clock frequency measurements and corresponding accuracy indicators to be transmitted through the packet-based network, and the clock frequency measurements being generated with increasing accuracy with respect to the first clock signal in a first phase of operation; and a second node to receive the clock frequency measurements and corresponding accuracy indicators from the first node via the packet-based network, the second node including signal synthesizer hardware to synthesize respective second clock signals from the received clock frequency measurements and corresponding accuracy indicators to retrieve the bit synchronous data, wherein, to generate the clock frequency measurements, the measurement hardware measures a number of counts during a predetermined period of time, and the accuracy indicator is a period of time for measuring the number of counts, and wherein, in the first phase of operation, the synthesizer hardware substantially reproduces the first clock signal at the second node based on incremental convergence of the second clock signals based on the received clock frequency measurements of increasing accuracy" as disclosed in claim 2.

"receiving a first clock signal for transmission through the packet-based network at the first node; repeatedly measuring, in a first phase, the first clock signal to obtain a plurality of frequency measurements of increasing accuracy at the first node; determining a corresponding accuracy indicator for each frequency measurement at the first node, the accuracy indicator being a time duration of measurement; individually transmitting each frequency measurement with its corresponding accuracy indicator through the packet-based network from the first node to the second node; receiving each frequency measurement and corresponding accuracy indicator at the second node; deriving, in the first phase, respective second clock signal signals from the frequency measurements and corresponding accuracy indicators at the second node, to

represent the first clock signal based on incremental converging of the second clock signals based on the received clock frequency measurements of increasing accuracy; and transmitting the derived second clock signals signal from the second node to user equipment connected to the second node" as disclosed in claim 3.

"receiving a first plurality of packets; determining a total time of transmission for each packet; identifying, from the first plurality of received packets, a first predetermined number of packets that have the first predetermined number of shortest total transmission times of the total transmission times of the plurality of received packets, the first predetermined number of packets identified being greater than one; and deriving the frequency of the transmitting clock by use of the identified first predetermined number of packets having the first predetermined number of shortest total transmission times " as disclosed in claim 4.

5. Additionally, all of the further limitations in claims 7, 8, 14, 15; 9, 10, 16, 17; 11, 18; 5, 6, 12, 13, 19, 20 are allowable since the claims are dependent upon independent claims.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew C. Lee whose telephone number is (571)272-3131. The examiner can normally be reached on Monday through Friday from 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andrew C Lee/
Examiner, Art Unit 2476
<10/20/2009:1Qy10>
/Ayaz R. Sheikh/
Supervisory Patent Examiner, Art Unit 2476